ISSN 23499842(Online), Volume 1, Special Issue 2(ICITET 15), March 2015
International Journal of Innovative Trends and Emerging Technologies

A NOVEL ENCODING METHOD FOR DSRC APPLICATION TO OBTAIN EFFICIENT

S.DEVIKA[1], S.LAVANYA[2]
[1]PG student, [2]Assistant professor, [1,2]VLSI Design, Department of Information and communication Engineering, Surya group of institutions, Vikravandi

Abstract : The dedicated short-range communication (DSRC) is an emerging technique to push the intelligent transportation system into our daily life. In this paper, we propose a novel encode method that can operate high efficiency in terms of HUR, and power consumption compared with existing method of DSRC application. The DSRC communication is a key enabling technology for the next generation of communication based safety application. The existing method consists of some limitations; this can be overcome by SOLS technique to obtain an efficient performance. The proposed method used to achieve efficient Hardware Utilization Rate is more than 57.14%. The simulation result of Model -sim indicates that it functions successfully and works at specified speed. The power consumption is reduced 112.58mW compared with existing works. As, expected the circuit can be easily integrated into DSRC application. In future by increasing the performance in any one of the DSRC application

1. INTRODUCTION

Nowadays, communication take place an important role to transfer the information from one place to another place without any degradation of data at the receiving side. The communication performs an essential role for different purpose at different environment application especially for transport purpose. The dedicated short range communication is a short to medium range ITS communications service that supports both public and private safety and private operation in roadside to vehicle and vehicle to vehicle communication modes. The vehicle to vehicle communication is only for broadcast purpose and the roadside to vehicle is generally broadcast with some two way transactions. DSRC was developed with a primary goal of enabling vehicular safety applications. DSRC is the only short-range wireless alternative today that provides: Fast Network Acquisition: Active safety applications require immediate establishment of communication. Low Latency: Active safety applications must execute in the smallest amount of time possible. High Reliability when Required: Active safety applications require high level of link reliability. Priority for Safety Applications: Safety applications on DSRC Interconnect-driven optimization [1] is an increasingly important step in high-performance design. Algorithms for buffer insertion have been successfully utilized to reduce delay in global interconnect paths; however, existing techniques only are given priority over non-safety applications. Interoperability: DSRC ensures interoperability, which is the key to successful deployment of active safety applications. Security and Privacy: DSRC provides safety message authentication and privacy. Communications-based active safety systems need a tightly controlled spectrum for maximized reliability. DSRC communications take place over a dedicated 75 MHz spectrum band around 5.9 GHz, allocated by the US Federal Communications Commission (FCC) for vehicle safety applications. The DSRC standards generally adopts two encode method to reach dc-balance, enhancing the signal reliability. Nevertheless, the coding-diversity between the FM0 and Manchester codes seriously limits the potential to design a fully reused VLSI architecture for both. The similarity-oriented logic simplification (SOLS) technique is proposed to overcome this limitation. This method improves the Hardware Utilization Rate (HUR) compared from the existing work and it also shows that none of the logic component is wasted during the process. The proposed technique consists of two core methods which are used to relocate the hardware resource to reduce the number of transistors and design fully reused hardware architecture. Finally the SOLS technique used to achieve efficient HUR increase the performance efficiently and reduction of power consumption. The objective is to achieve 100% Hardware Utilization Rate and to achieve efficient performance & to reduce power. DSRC applications are DSRC enables the most reliable, high speed vehicle-based technology for crash prevention safety applications. It also provides for a broad cross-section of dedicated connectivity options for surface transportation safety. DSRC based communications serves as the basis for connected vehicle safety and mobility application integration. Potential DSRC Transportation Applications for Public Safety and Traffic Management consists of following advantages: Emergency warning system for vehicles .Cooperative Adaptive Cruise Control. Cooperative Forward Collision Warning.

.II. RELATED WORK

optimize delay and timing slack. With the continually increasing ratio of coupling capacitance to total capacitance and the use of aggressive dynamic logic circuit families, noise analysis and avoidance is becoming a major design bottleneck. Hence, timing

and noise must be simultaneously optimized to achieve maximum performance. A buffer minimization problem [2] is formulated. Although it is NP-hard in general, it can be solved linearly when buffers are required on multi fan-out nodes. We also consider the case when buffers are inverters, where phase assignment needs to be done with buffer insertion. Dedicated Short-Range Communication (DSRC) is a key enabling technology [3]for the next generation of communication-based safety applications. One aspect of vehicular safety communication is the routine broadcast of messages among all equipped vehicles. Therefore, channel congestion control and broadcast performance improvement are of particular concern and need to be addressed in the overall protocol design. TSMC CMOS 0.35 μm 2P4M process technology [4]. The simulation result of HSPICE indicates that it functions successfully and works at 200-MHz speed. The average power consumption of the circuit under room temperature is 549 μW. The total core area is 70.7 μm × 72.2 μm. As expected, the circuit can be easily integrated into Radio Frequency Identification (RFID) application.[5] the DSRC spectrum is organized into several channels. IEEE 1609.4 defines a time-division scheme for DSRC radios to alternately switch within these channels to support different applications concurrently. We describe the main features of IEEE 1609.4 in detail and discuss the main concerns with the original protocol design. In particular, we focus on those issues that can have a significant impact on vehicle safety communications. joint coded-FSK detection scheme[6] with low complexity benefit can outperform the conventional separated coded-FSK detection scheme. It is due to the joint scheme with time diversity gain to enhance the detection performance. Moreover, the proposed joint algorithms with floating-point and fixed-point designs are verified in the software-defined-ratio (SDR) platform. An analytical model for the reliability of a dedicated short-range communication (DSRC) control channel (CCH) to handle safety applications in vehicular ad hoc networks (VANETs) is proposed [7]. Specifically, the model enables the determination of the probability of receiving status and safety messages from all vehicles within a transmitter's range and vehicles up to a certain distance, respectively. The remainder of this paper is organized as follows. Section II related work describes the coding principles for without SOLS techniques .The proposed VLSI architecture design using SOLS technique is reported in Section III. Two core methods of SOLS technique, area compact retiming and balance logic-operation sharing, are described in this section. The experiment results and discussion are presented in Section IV. This section focuses on an objective evaluation between this design and existing articles of Manchester and FM0 encoders. Finally, the conclusion is given in Section V.

c) Hardware architecture of limitation analysis

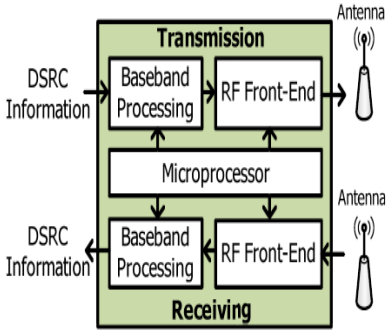
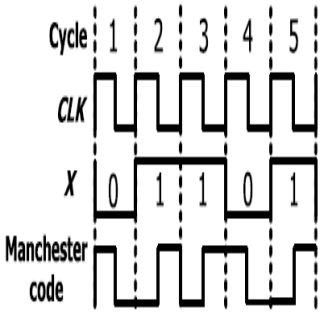
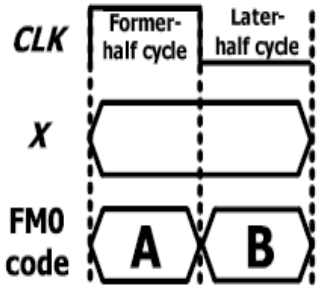


Fig. 2.1. System architecture of DSRC transceiver.

A) Manchester Code



B) FM0 Code



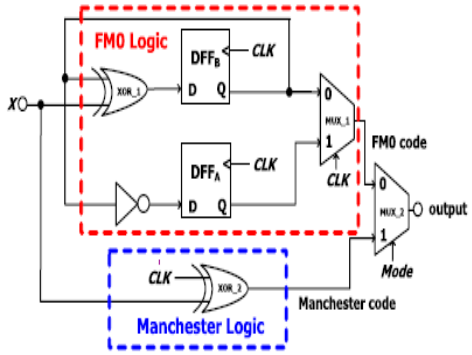


Fig. 2.2 Hardware architecture

Table I

HUR of FM0 and Manchester encodings Without SOLS

Coding	Active components(transistor count)/ Total components(transistor count)	HUR
FM0	6(44)/7(50)	85.71 %
Manchester	2(12)/7(50)	28.57 %
Average	4(28)/7(50)	57.14 %

III.VLSI ARCHITECTURE DESIGN USING SOLS TECHNIQUE

The SOLS technique is classified into two parts: Area-compact retiming, Balance logic-operation sharing.

A) Area Compact Retiming

Area compact retiming method is used for designing FM0 encoding logic. Area compact retiming is a method to perform the same function even any changes or any modification in the location of logic components. This method is used to reduce the number of transistor from the existing method. The FM0 logic in the hardware architecture of existing method is simply shown in Fig.4.1. The logic for A(t) and the logic for B(t) are the Boolean functions to derive A(t) and B(t), where the X is omitted for a concise representation. For FM0, the state code of each state is stored into DFF_A and DFF_B.

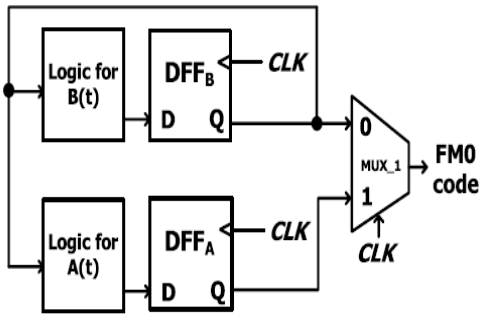


Fig. 3.1 FM0 encoding without area-compact retiming

According to equation (2) and (3), the transition of state code only depends on B(t − 1) instead of both A(t − 1) and B(t − 1). Thus, the FM0 encoding just requires a single 1-bit flip-flop to store the B(t−1). If the DFF_A is directly removed, a non synchronization between A(t) and B(t) causes the logic fault of FM0 code. To avoid this logic-fault, the DFF_B is relocated right after the MUX_1, as shown in below Fig.4.2, where the DFF_B is assumed to be positive-edge triggered.

At each cycle, the FM0 code, comprising A and B, is derived from the logic of A(t) and the logic of B(t), respectively. The FM0 code is alternatively switched between A(t) and B(t) through the MUX_1 by the control signal of the CLK. In Fig. 4.1, the Q of DFF_B is directly updated from the logic of B(t) with 1-cycle latency. In Fig. 4.2, when the CLK is logic-0, the B(t) is passed through MUX_1 to the D of DFF_B. Then, the upcoming positive-edge of CLK updates it to the Q of DFF_B.

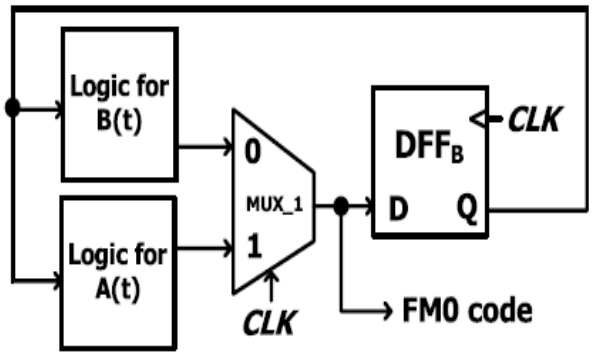


Fig.3.2 FM0 encoding with area-compact retiming

Table II

Transistor Count for Various Logic Functions

Function	Transistor Count
Flip flop, edge triggered dynamic D with reset	12
MUX 2 input	6
NOR 2 input	4
NOT	2
XOR 2 input	6
XNOR 2 input	8

B) Balance Logic-Operation Sharing

The Manchester encoding can be derived from the simple X ⊕ CLK, and it can be written as, X ⊕ CLK = X CLK + X CLK. The logic for A(t)/X and the logic for B(t)/X obtained based on the following process . The A(t) can be derived from an inverter of B(t − 1), and X

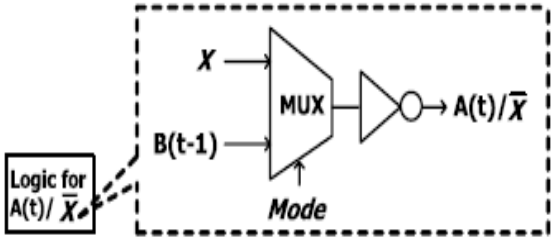


Fig.3.3 Balance logic-operation sharing of A(t) and X

The X can be also interpreted as the X ⊕ 0, and thereby the XOR operation can be shared with Manchester and FM0 encodings. As a result, the logic for B(t)/X is shows, where the multiplexer is responsible to switch the operands of B(t−1) and logic-0. This architecture shares the XOR for both B(t) and X, and thereby increases the HUR.Furthermore, the multiplexer can be functionally integrated into the relocated DFF_B from area-compact retiming technique. The CLR is the clear signal to reset the content of DFF_B to logic-0. The DFF_B can be set to zero by activating CLR for Manchester encoding. When the FM0 code is adopted, the CLR is disabled, and the B(t −1) can be derived from DFF_B. Hence, the multiplexer can be totally saved, and its function can be completely integrated into the relocated DFF_B

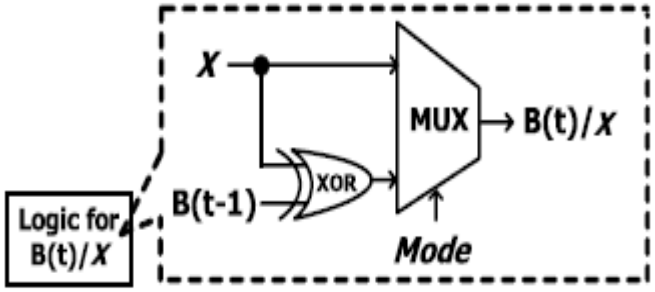


Fig.3.4 Balance logic-operation sharing of B(t) and X

The proposed VLSI architecture of FM0/Manchester encoding using SOLS technique is obtained based on the two core methods

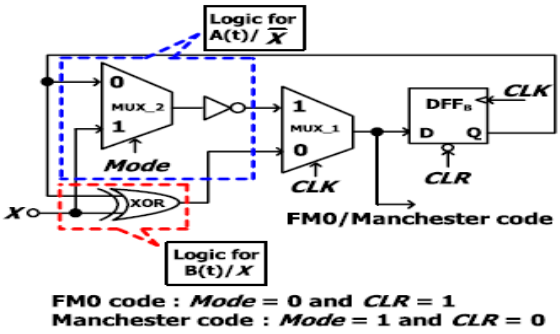
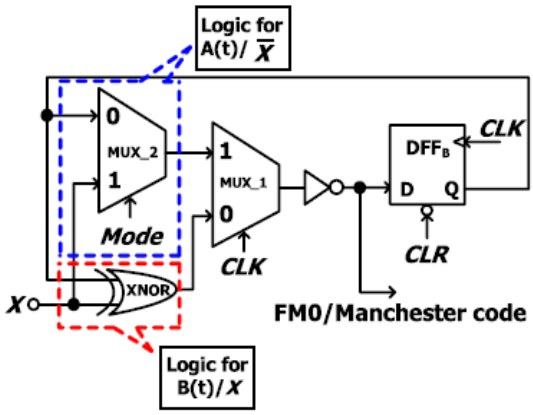


Fig.3.5 Unbalance computation time between A(t)/X and B(t)/X

To alleviate this unbalance computation time, the architecture of the balance computation time between A(t)/X and B(t)/X is shown in Fig.4.9. The XOR in the logic for B(t)/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for A(t)/X. This shared inverter is relocated backward to the output of MUX_1. Thus, the logic computation time between A(t)/X and B(t)/X is more balance to each other. The adoption of FM0 or Manchester code depends on Mode and CLR. In addition, the CLR further has another individual function of a hardware initialization. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization. To avoid this conflict, both

Mode and CLR are assumed to be separately allocated to this design from a system controller. Whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings. Therefore, the HUR of the proposed VLSI architecture is greatly improved



FM0 code : *Mode* = 0 and *CLR* = 1
Manchester code : *Mode* = 1 and *CLR* = 0

Fig.3.6 Balance computation time between A(t)/X and B(t)/X

Table III

HUR of FM0 and Manchester encodings with SOLS

Coding	Active components(transistor count)/ Total components(transistor count)	HUR
FM0	5(34)/5(34)	100%
Manchester	5(34)/5(34)	100%
Average	5(34)/5(34)	100%

IV. SIMULATION AND OUTPUT

I) Output Waveform for Manchester Code without SOLS Method

A. Manchester Code Output Waveform

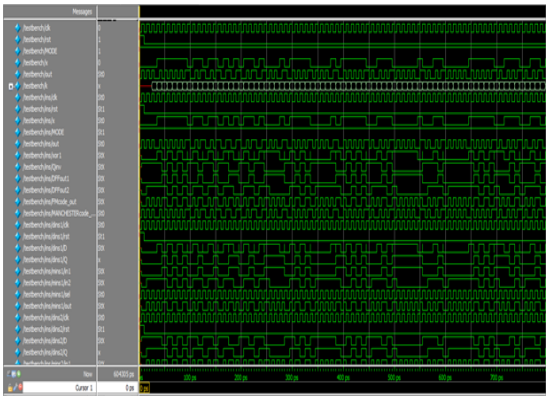


Fig 4.1 Implementation of Manchester Code Output Waveform

B.FM0 Code Output Waveform

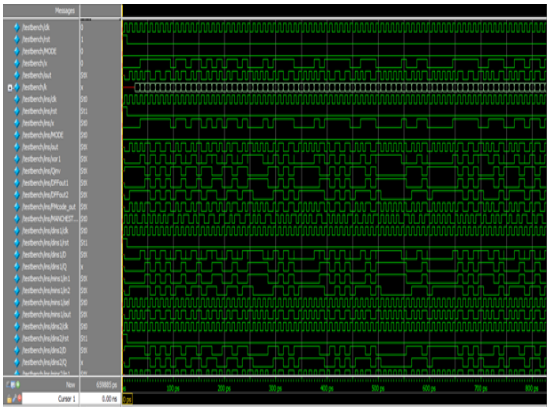


Fig *4.2* Implementation of FM0 Code Output Waveform

C .Power Analyzer

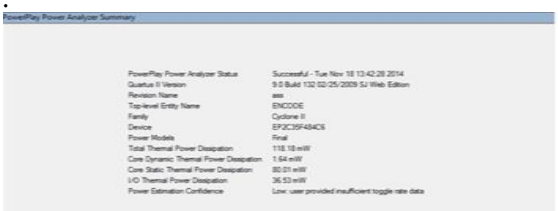


Fig *4.3* Implementation of power analyzer

II) Output Waveform for Manchester Code with SOLS Method

A. anchester Code Output Waveform

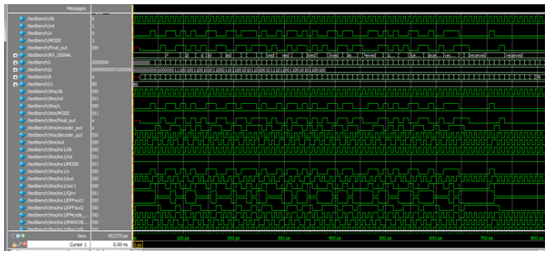
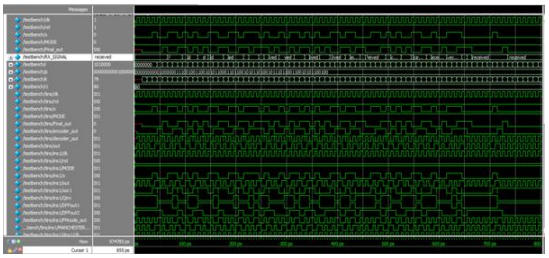


Fig *4.4* Implementation of Manchester Code Output Waveform

B. M0 Code Output Waveform



III) Comparison of without sols method and with sols method

Table IV

METHOD	HUR PERCENTAGE	POWER CONSUMPTION
Without SOLS Technique	57.14%	118.18mW
With SOLS Technique	100%	112.58mW

Fig *4.5* Implementation of FM0 Code Output Waveform

C .Power Analyzer

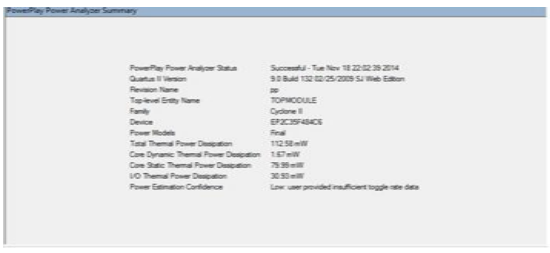


Fig *4.6* Implementation of power analyzer

VI. CONCLUSION

The fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. In this project the novel encoding method is intended to achieve Hardware utilization rate is about 100% compared from the 57.14% of existing work. The coding-diversity between FM0 and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. The proposed SOLS technique eliminates this limitation on hardware utilization of existing method by two core techniques: area compact retiming and balance logic-operation sharing. The proposed method not only achieves the HUR but also used to obtain the efficient performance and reduction of power consumption and hence with improved performance.

REFERENCES

[1] Khalid Abdel Hafeez, "Performance Analysis And Enhancement Of The DSRC For Vanet's Safety Applications" Student Member, IEEE, Lian Zhao, Senior Member, IEEE, Bobby Ma, Senior Member, IEEE, and Jon W. Mark, Life Fellow, IEEE vol. 62, No. 7, Sep 2013

[2] Y.-C. Hung, M.-M. Kuo, C.-K. Tung, and S.-H. Shieh, "High-speed CMOS chip design for Manchester and Miller encoder," in *Proc. Intell. Inf. Hiding Multimedia Signal Process.*, Sep. 2009, pp. 538–541.

[3] Qi Chen, Daniel Jiang, Luca Delgrossi "IEEE 1609.4 DSRC Multi-Channel Operations and Its Implications on Vehicle Safety Communications" Mercedes-Benz Research & Development North America, Inc

[4] J.-H. Deng, F.-C. Hsiao, and Y.-H. Lin, "Top down design of joint MODEM and CODEC detection schemes for DSRC coded-FSK systems over high mobility fading channels," in *Proc. Adv. Commun. Technol.* Jan. 2013, pp. 98–103.

[5] J. Daniel, V. Taliwal, A. Meier, W. Holfelder, and R. Herrtwich, "Design of 5.9 GHz DSRC-based vehicular safety communication," *IEEE Wireless Commun. Mag.*, vol. 13, no. 5, pp. 36–43, Oct. 2006.

[6] Hai Zhou and Adnan Aziz, "Buffer Minimization in Pass Transistor Logic" IEEE transactions on computer-aided design of integrated circuits and systems, vol. 20, no. 5, may 2001

[7]Charles J. Alpert, Member, IEEE, Anirudh Devgan, Member, IEEE, and Stephen T. Quay, "Buffer Insertion for Noise and Delay Optimization" C. J. Alpert is with the IBM Austin Research Laboratory, Austin, TX 78758 USA (e-mail: alpert@austin.ibm.com).