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HIGH SPEED PARALLEL ARCHITECTURE FOR FBMC/OQAM TRANSMITTER

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Abstract

The Filter-Bank Multi-Carrier with Offset Quadrature Amplitude Modulation (FBMC/OQAM) is considered by recent research projects as a key enabler for the future 5G air interface. It exhibits better spectrum shape and improves mobility support compared to Orthogonal Frequency-Division Multiplexing (OFDM). Therefore, the availability of efficient hardware implementations becomes of high interest. The proposed architecture provides a complexity reduction of 40 to 50% in terms of computational and memory resources with respect to a typical FBMC/OQAM transmitter. The parallel architectures have been proposed in an effort to reduce power consumption as well as to relax timing constraints. Exploiting parallelism with 4-way parallel architecture enables to keep throughput constraint at time, lower clock speeds, whereas it may increase the hardware resources by a factor. Multi-band orthogonal frequency-division multiplexing (MB-OFDM) is one of 4G ultra wideband (UWB) radio standards, which provides high-speed connectivity in a wireless personal area network (PAN). In this project, offset modulation combined FMBC pipelined FFT architecture has been proposed for OFDM-based WPAN applications. Highly parallelized FBMC/OQAM transmitter is designed and its complexity and performance gap over OFDM is well proved using FPGA synthesis. Analytical FPGA synthesis results of the proposed cyclic prefix less FBMC transmitter shows significant throughput enhancement over OFDM methods. To reduce the overall system design complexity multiplier less IFFT and PPN filter networks is proposed.

Index terms: OFDM, FBMC, IFFT and PPN filter

1. Introduction

In telecommunications, 4G is the fourth generation of cellular wireless standards. It is a successor to 3G and 2G families of standards. Multi-band orthogonal frequency-division multiplexing (MB-OFDM) is one of 4G ultra wideband (UWB) radio standards, which provides high-speed connectivity in a In wireless personal area network (PAN) with specification of the data rates from 53.3 to 480 Mbps . Due to the high data rates, the MB-OFDM standard requires to process large amount of computations in very short time; its modem has to compute one symbol that consists of 165 complex numbers in every 312.5 ns. Even though its performance requirement results in large hardware complexity, a low power design with small chip size is absolutely essential for applying this technology to portable handheld devices. Also, an operating frequency of a circuit is one of the dominant factors that determine power consumption.

In MB-OFDM, the standard specification defines a sampling frequency of 528 MHz Such high frequency is problematic when we use it as a system clock speed; it consumes too much power and it is hard to implement due to timing constraints. Therefore, parallel architectures have been proposed in an effort to reduce power consumption as well as to relax timing constraints. Exploiting parallelism with 4-way parallel architecture enables to keep throughput constraint at time, lower clock speeds, whereas it may increase the hardware resources by a factor. Despite of the increased hardware resources, it is possible to reduce power consumption as well as to relax timing constraints due to two reasons. First, X way parallel architecture compensates for X times longer gate delays. Therefore, the parallel hardware can operate at reduced supply voltages and consequently consume less power. However, supply voltage scaling is beyond this project scope: our work focused on high level resource optimization. Second, a resource efficient design, on which this paper focuses, is able to avoid the linear i.e., times, resource increments.

In telecommunications, frequency division multiplexing (FDM) is a technique by which the total bandwidth available in a communication medium is divided into a series of non-overlapping frequency sub-bands, each of which is used to carry a separate signal. This allows a single transmission medium such as a cable or optical fiber to be shared by many signals. An example of a system using FDM is cable television, in which many television channels are carried simultaneously on a single cable. Where frequency-division multiplexing is used as to allow multiple users to share a physical communications channel, it is called frequency-division multiple access (FDMA). FDMA is the traditional way of separating radio signals from different transmitters. By interleaving the symbols across sub-bands, the UWB system can still maintain the same transmit power as if it were using the entire bandwidth. By using smaller sub-bands to transmit the information, the processing bandwidth for the receiver can be reduced, thereby lowering the complexity of the design, reducing the power consumption of the radio, lowering the overall solution cost, and improving spectral flexibility and worldwide compliance. In MB-OFDM, the standard specification defines a sampling frequency of 528 MHz. Such high frequency is problematic when we use it as a system clock speed; it consumes too much power and it is hard to implement due to timing constraints. Therefore, parallel architectures have been proposed in an effort to reduce power consumption as well as to relax timing constraints.

2. Related Work

In the analysis and design of OFDM/OQAM systems based on filterbank theory, Cyrille Siclet, Pierre Siohan, and Nicolas Lacaille carried out discrete analysis of the orthogonal frequency division multiplex/offset QAM (OFDM/OQAM) multicarrier modulation technique [1], leading to a modulated

Trans multiplexer. The orthogonal conditions of the modulated Trans multiplexer they have just obtained naturally depend on the analysis and synthesis filter banks. To get a compact representation of a system, they use the poly phase approach, which leads us to IFFT-based implementations, to the input–output relation and, finally, allows us to get the mathematical orthogonal conditions. The conditions of discrete orthogonal are established with respect to the poly phase components of the OFDM/OQAM [6] prototype filter, which is assumed to be symmetrical and with arbitrary length. For accurate implementation of the OFDM/OQAM modulator and demodulator, stage based inverse fast Fourier transform were used. Non-orthogonal prototypes create inter symbol and inter channel interferences (ISI and ICI) that, in the case of a distortion-free transmission, are expressed by a closed-form expression.

A large set of design examples is presented for OFDM/OQAM systems with a number of subcarriers going from four up to 2048, which also allows a comparison between different approaches to get well-localized prototypes. Both modulator, and demodulator, which are fully, based on the IFFT leads complexity issues. The main limitation of this implementation is that the performance in terms of BER analyzes is not carried out. This method requires exactly satisfied the discrete orthogonal conditions else will create ISI and ICI.

Gharba Mohamed,Hao Lin, Pierre Siohan [3] proposed a novel analysis of the sensitivity of an important class of filter bank multicarrier (FBMC) systems to time and frequency offsets called Impact of time and carrier frequency offsets on the FBMC/OQAM modulation scheme. And they point out an important interference model, which is crucial for our later analysis in the case of de-synchronization. Since the considered impairments are related to analog front end imperfections, they start by a description in continuous time and we shift afterwards to the digital domain to be in line with our simulations that are run in discrete-time For the FBMC system under consideration the mapping for each sub-carrier uses offset quadrature amplitude modulation (OQAM) constellations.

They developed a general reduced-rate OFDM transmission scheme for ICI self-cancellation over high-mobility fading channels. By transmit and receive processing, we have transformed the original OFDM system into an equivalent one with fewer subcarriers and significantly reduced ICI. In particular, general structure of transmit and receive processing matrices to guarantee a common average SIR over all equivalent sub channels in the transformed OFDM system. Here they assuming that the time offset (TO) and carrier frequency offset (CFO) are less than the symbol duration and sub-carrier frequency spacing, respectively, they derive exact analytical expressions of the interference power resulting from TO and CFO. Our theoretical results are confirmed by simulations for a large set of prototype filters. Furthermore, in the case of perfectly orthogonal prototype filters, we establish the link with a simple expression that up to now was left unused. Overall the impact of time and carrier frequency offsets over filter bank multicarrier (FBMC) system is analyzed and its robustness is well proved. And finally it is proved that FBMC is generally less sensitive to synchronization errors than OFDM system. However the problems over integrated FBMC design are not analyzed.

In the paper of techniques for Suppression of Inter Carrier Interference in OFDM Systems [4] proposed by John G. Proakis, Tiejun (Ronald) Wang and James R.Zeidler, they considered OFDM system with frequency selective time varying fading channel model and assume perfect channel state information is not available at the receiver. The channel frequency response $ht\ k[n]$ and time domain impulse response $hl\ t[n]$ are estimated at the receiver end by inserting pilots at some of the subcarriers and thus, estimating the frequency response of the channel at selected frequencies. This system is strongly motivated by the similarities between ICI distortion in OFDM systems and ISI distortion in single carrier systems, and considers an MMSE based detection technique to suppress ICI. By taking both ICI and additive noise into account, the MMSE-based OFDM detection technique is superior to the conventional OFDM detection scheme described above.

By combat the ICI distortion caused by Doppler-spread of the time-varying fading channels, the MMSE-based OFDM receiver structure was used as a detection technique. The system performance is affected by the linear time variation of the channel. The channel estimations fully relies on unique detection techniques leads complexity.

3. Proposed Work

FDMA (frequency division multiple access) is the channel access method used in multiple-access protocols as a channelization protocol. FDMA gives users an individual allocation of one or several frequency bands, or channels. It is particularly commonplace in satellite communication. FDMA, like other Multiple Access systems, coordinates access between multiple users. The UWB spectrum is divided into 14 bands, each with a bandwidth of 528 MHz. The first 12 bands are then grouped into 4 band groups consisting of 3 bands. The last two bands are grouped into a fifth band group. A sixth band group is also defined within the spectrum of the first four, consistent with usage within worldwide spectrum regulations. At least one of the band groups (BG1 - BG6) shall be implemented. This standard specifies a Multiband Orthogonal Frequency Division Modulation (MBOFDM) scheme to transmit information [2]. A total of 110 sub-carriers (100 data carriers and10 guard carriers) are used per band to transmit the information. In addition, 12 pilot subcarriers allow for coherent detection.

Frequency-domain spreading, time-domain spreading, modulation and forward error correction (FEC) coding are used to vary the data rates. The coded data is spread using a time-frequency code (TFC). This standard specifies three types of time-frequency codes (TFCs). One where the coded information is interleaved over three bands, referred to as Time-Frequency Interleaving (TFI); one where the coded information is interleaved over two bands, referred to as two-band TFI orTFI2.

For the sake of simplicity, a MB-OFDM system consisting only three bands is described herein. How the OFDM symbols are transmitted in a MB-OFDM system. In this example, it has been implicitly assumed that the time-frequency coding (TFC) [7] is performed across just three OFDM symbols; however, in

practice, the TFC pattern can have a much longer periodicity. MULTI-BAND orthogonal frequency-division multiplexing (MB-OFDM) is one of ultra wideband (UWB) radio standards, which provides high-speed connectivity in a wireless personal area network (PAN) with specification of the data rates from 53.3 to 480 Mbps. Due to the high data rates, the MB-OFDM standard requires to process large amount of computations in very short time. Even though its performance requirement results in large hardware complexity, a low power design with small chip size is absolutely essential for applying this technology to portable handheld devices.

This technology promises to deliver data rates that can scale from a data rate of 110 Mb/s at a distance of 10 meters up to a data rate of 480 Mb/s at a distance of 2 meters in realistic multi-path environments all while consuming very little power and silicon area. It is expected that UWB devices will be able to provide low cost solutions that can satisfy the consumers need for data rates as well as enable new consumer market segments. The previous literature presented only one resource optimization technique which sacrifices the overall system performance although the degradation is negligible.

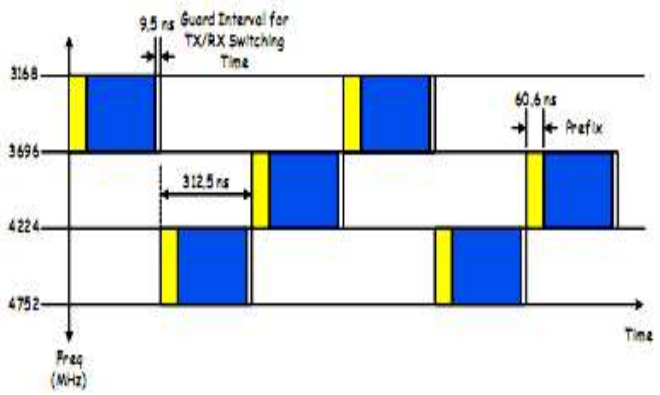

Figure 1: Coding for an MB-OFDM system

In a MB-OFDM system, a guard interval (9.5 nanoseconds) is appended to each OFDM symbol and a zero-padded prefix (60.6 nanoseconds) is inserted at the beginning of each OFDM symbol. The guard interval ensures that there is sufficient time for the transmitter and receiver to switch to the next carrier frequency. A zero- padded prefix provides both robustness against multi-path and eliminates the need for power back-off at the transmitter. More details about the zero-padded prefix will be described in a later section.

4. Architecture For FBMC WITH OQAM

In OFDM, information bits to be transmitted are first modulated to generate complex In-phase I and Quadrature Q components. A maximum of M QAM symbols are modulated, corresponding to the number of active sub-carriers of OFDM. Then, an IFFT of length M (IFFTM) is computed and a block of M complex samples is generated in time domain as shown in Figure 2. Unused sub-carriers are padded to zero at the input of the IFFT. The baseband OFDM modulation in discrete time domain can be written. A Cyclic Prefix (CP) is inserted at the beginning of a block (OFDM symbol) to avoid inter-symbol interference caused by the delay spread of a multipath channel at a noticeable cost in spectral efficiency.

The first unit of the proposed OFDM modulator architecture is the QAM mapper which is typically implemented through a Look-Up Table (LUT), supporting up to 64-QAM, as specified in the Long Term Evolution (LTE) standard. The R22 SDF architecture was chosen for the IFFT block thanks to its low complexity, its minimum memory requirement and its pipelined structure. The devised architecture for the IFFT uses the Decimation in Frequency (DIF) decomposition which results in output samples in bit reversal order.

MB-OFDM defines two constellation mapping schemes: QPSK and DCM modulations. The QPSK spreads data into several subcarriers and the DCM requires data reordering. The spreading and reordering processes involve non-trivial amount of buffer storages and also latency. Conventionally those processes are done as separate phases: interleaving first and then spreading or reordering. But, we can unify the spreading and the (inverse)-reordering with the (de)interleaving process. With the proposed inter leaver architecture, we can perform he spreading before the interleaving process by fully utilizing array cells of our inter leaver. The DCM (inverse)-reordering attern can be combined into the (de)interleaving process so hat the reordering is done in parallel with the interleaving process. This way removes the additional buffer storages as well as latency for the spreading and the (inverse)-reordering. Since DCM-decamped bit streams are inverse-reordered, which is more storage demanding than the spreading, in a group of 100 soft decision bits basis, the storage reduction is 300-bits: 100 soft decision bits 3-bits per soft decision bit. To satisfy throughput demands of its output consuming units, the inter leaver needs to be implemented with a highly unfolded inter-cell network: 10 and 20 times unfolding for the QPSK and DCM modulations, respectively. A serial implementation requires a few cells to have wide input multiplexers for changing inter-cell connections according to various interleaving parameters determined by data rates. In contrast, such cells are dominant with the highly unfolded inter-cell network.

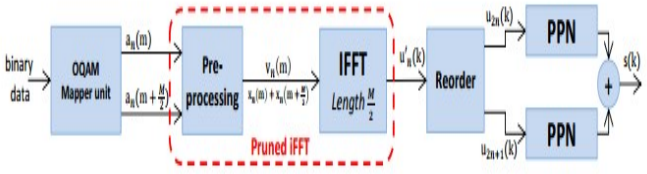

Figure 2: Optimized FBMC/OQAM hardware architecture using pruned IFFT algorithm

The number of input ports of each cell-input multiplexer increases from 2 to around 4, in case of the unified (de)inter leaver, due to 10/20 times unfolding. Basically, the cell has a symmetric structure. With this structure, a datum of one flip-flop (e.g., FF0) is moved to a horizontally connected cell for storing inputs to be interleaved (input-phase). After a block of inputs is stored, in turn, the stored datum is moved in a vertical direction (output-phase).At the same time, another flip-flop (e.g., FF1) takes the input storing process for the next incoming input block in a horizontal direction. De interleaving can be done simply by moving data in the opposite directions. Therefore, one flip-flop (FF0) needs just a

two-input multiplexer: one input for inter-cell move and another for intra cell move.

To reduce the multiplexing costs with the proposed cell structure, instead of changing inter-cell data-moving directions between input and output-phases, one flip-flop moves its datum to another flip-flop, i.e., intra-cell move, once at the beginning of output phase. Because inter-cell data-moving direction is now fixed, this way eliminates cell-output multiplexers. In fact, inter cell connections are consistent across all interleaving parameters in input-phase of interleaving and output-phase of de interleaving. Therefore, one flip-flop (FF0) needs just a two-input multiplexer: one input for inter-cell move and another for intra cell move.

This cyclic prefix both preserves the orthogonal of the subcarriers and prevents ISI between successive OFDM symbols. Therefore, equalization at the receiver is very simple. This often motivates the use of OFDM in wireless systems. Between consecutive OFDM signals a guard period is inserted that contains a cyclic extension of the OFDM symbol. The OFDM signal is extended over a period Δ so that,

$$s(t) = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} x_k e^{j2\pi f_k t}, \qquad -\Delta < t < NT.$$

The signal then passes through a channel, modelled by a finite-length impulse response [5] limited to the interval $[0, \Delta_h]$. If the length of the cyclic prefix Δ is chosen such that $\Delta > \Delta_h$ the received OFDM symbol evaluated on the interval $[0, NT]$, ignoring any noise effects, becomes

$$r(t) = s(t) * h(t) = \frac{1}{\sqrt{N}} \sum_{k=0}^{N-1} H_k x_k e^{j2\pi f_k t}, \qquad 0 <$$

where

$$H_k = \int_0^{\Delta_h} h(\tau) e^{j2\pi f_k \tau} d\tau$$

is the Fourier transform of $h(t)$ evaluated at the frequency f_k. Note that within this interval the received signal is similar to the original signal except that $H_k x_k$ modulates the subcarrier instead of x_k. In this way the cyclic prefix preserves the orthogonal of the subcarriers.

5. Experimental Result

. The step is called "technology mapping & optimization" which maps the internal representation to an optimized gate level representation using the technology library cells based on design constraints. Input port of the design under test to input of one internal flip-flop Output of an internal flip-flop to input of another flip-flop Output of an internal flip-flop to output port of the design under test. A combinational path connects the input and output ports of the design under test. The delays of combinational gates, setup time of flip-flops and Clock-To-Q values are derived from the LSI_10k library file that was used for the mapping step during synthesis.

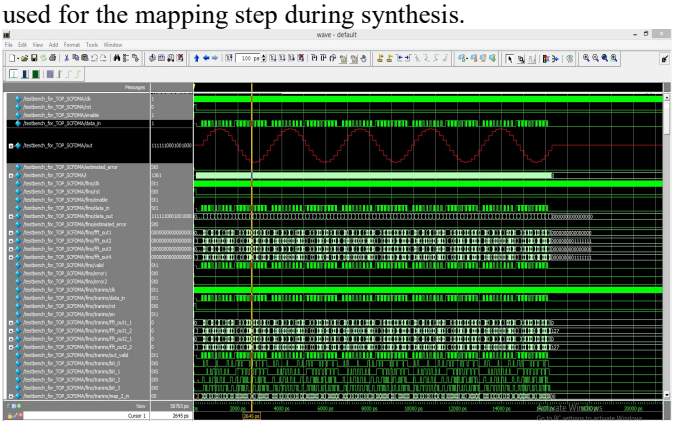

Figure 3: Simulated output of FBMC

A primary objective of this project was to develop a synthesizable model for the FFT algorithm. Synthesis is the process of converting the register transfer level (RTL) representation of a design into an optimized gate-level net list. This is a major step in ASIC design flow that takes an RTL model closer to a low-level hardware implementation. To enforce the synthesis tool to create the most compact net list, the area of the gate level net list was constrained to zero during the synthesis process. As a result, the only constraint violation, which is expected, is related to the area. It also uses the area parameter associated with each cell in the LSI_10K library file, to calculate the total combinational and sequential area of the net list. The total area of the gate level net list is unknown since it depends on total area of interconnects, which itself is a function of the wiring load model used in physical design. The total cell area in the net list is reported as 22978 units, which is the sum of combinational and sequential areas as shown in Table 1.

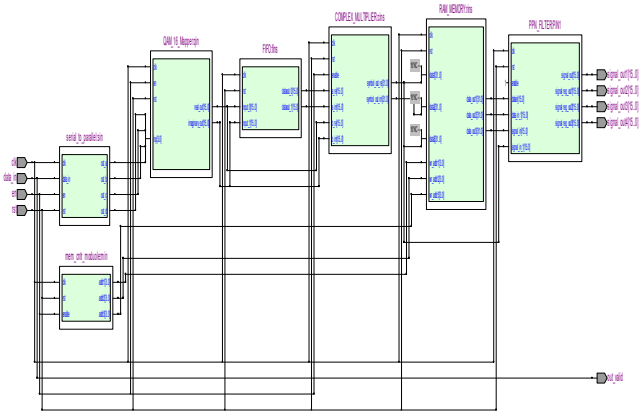

Figure 4: RTL Schematic report.

The last DC command in the script developed in previous section, instructs the tool to report the path with the worst timing. In this case, the path with the worst timing is a combinational path of type two. The delay associated with this path is the summation of delays of all combinational gates in the path plus the Clock-To-Q delay of the originating flip-flop, which was calculated as 24.09ns. By considering the setup time of the destination flip-flop in this path, which is 0.85ns, the 40MHz clock signal satisfies the worst combinational path delay. The delays of combinational gates, setup time of flip-

flops and Clock-To-Q values are derived from the LSI_10k library file that was used for the mapping step during synthesis. Designs using the Register-Transfer Level as shown in figure 4 specify the characteristics of a circuit by transfer of data between the registers, and also the functionality; for example Finite State Machines. An explicit clock is used. RTL design contains exact timing possibility; and data transfer is scheduled to occur at certain times.

Transmitter Type	Area	Speed
Existing system of OFDM	160 with 8MUL	175.38MHz
Proposed system of FBMC	181 with 4MUL	378.5MHz

Table 1: Trade off analyzes of OFDM Vs FBMC

6. Conclusion

In this project, offset modulation combined FMBC pipelined FFT architecture has been proposed for OFDM-based WPAN applications. Highly parallelized FBMC/OQAM transmitter is designed and its complexity and performance gap over OFDM is well proved using FPGA synthesis. Analytical FPGA synthesis results of the proposed cyclic prefix less FBMC transmitter shows significant throughput enhancement over OFDM methods. In this project carried out FFT with combined FBMC pipelined FFT architecture. To reduce the complexity further multiplier less shift based accumulation has been proposed. In order to reduce overall latency of accumulation prefix based arithmetic computation has to be added.

7. References

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